IN THE CLAIMS

Please amend the specification as follows.

1. (Currently Amended) A parallel counter comprising:

at least five inputs for receiving ~~a binary number as~~ a plurality of binary inputs;

at least three outputs for outputting binary outputs ~~code~~ indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of ~~binary~~ outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein the logic circuit comprises at least one of:

elementary OR symmetric function logic comprising at least one of ~~comprises the result of~~ OR logic for combining binary inputs to generate a binary output which is high if and only if m [[>]] ≥1 ~~or~~ , AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m [[>]] ≥k, and

~~the~~ elementary EXOR symmetric function logic comprising at least one of ~~comprises the result of~~ EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m [[>]] ≥1 and the number of high inputs is an odd number, ~~or~~ AND logic for combining sets of ~~one or more~~ binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m [[>]] ≥ k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.

2.-3. (Canceled)

4. (Currently Amended) A parallel counter according to claim 1 wherein said elementary XOR symmetric function logic includes ~~logic circuit is arranged to~~ at least one of:

logic to generate the ~~first and~~ least significant bit of the binary output ~~by EXOR logic combining the binary inputs~~; and

logic to generate the $(i+1)^{th}$ binary output ~~by~~ including logic to AND logic ~~combining~~ combine 2^i of the binary inputs in each set and EXOR logic to combine ~~combining~~ the result of the AND logic combinations, where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance of a binary output ~~, each set being unique and the sets covering all possible combinations of binary inputs~~.

5.-7. (Canceled)

8. (Currently Amended) A parallel counter according to claim1 wherein said elementary OR symmetric function logic ~~circuit is arranged~~ includes logic to logically AND 2^{N-1} of the binary inputs in each set in the generation of the N^{th} binary output as the elementary OR symmetric function of the binary inputs, where N is the number of binary outputs and the N^{th} binary output is the most significant ~~, each set being unique and the sets covering all possible combinations of binary inputs~~.

9. (Canceled)

10. (Currently amended) A parallel counter according to claim 1 wherein said elementary XOR symmetric function logic ~~circuit~~ is adapted ~~arranged~~ to generate a first binary output as an elementary EXOR symmetric function of the binary inputs, and said elementary OR symmetric function logic is adapted to generate an N^{th} binary output as an elementary OR symmetric function of the binary inputs.

11. (Currently Amended) A parallel counter according to claim 1 wherein said elementary OR symmetric function logic includes intermediate logic ~~circuit is arranged~~ to generate ~~two~~ a plurality of possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, where N is the number of binary outputs, the sets used for each possible binary output being of ~~two~~ different sizes which are a

function of the binary output being generated; and ~~said logic circuit including~~ selector logic to select one of the possible binary outputs based on ~~a~~ at least one more significant binary output value.

12. (Currently Amended) A parallel counter according to claim 11 wherein said intermediate logic ~~circuit is arranged~~ includes logic adapted to generate ~~the~~ two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively, and said selector logic being adapted ~~arranged~~ to select one of the possible binary outputs based on the N^{th} binary output value.

13. (Currently Amended) A parallel counter according to claim 1 wherein said elementary OR symmetric function logic ~~circuit includes~~ and said elementary EXOR symmetric function logic include a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary OR or EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

14.-20. (Canceled)

21. (Currently Amended) A logic circuit for multiplying two N bit binary numbers, the logic circuit comprising:

array generation logic ~~for performing a first stage of logical combining by performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combinations comprising an array of binary values, and for performing a second stage of logical combining by logically combining AND combinations~~ adapted to generate an array of logical combinations of bits of binary numbers ~~in which the maximal depth of the array is below N bits~~;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter ~~according to claim 1, 4, 8, 10, 11, 12, or 13~~ comprising:

at least five inputs for receiving a plurality of binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the outputs as elementary OR or EXOR symmetric functions of the inputs, wherein the logic circuit comprises at least one of:

elementary OR symmetric function logic comprising at least one of OR logic for combining binary inputs to generate a binary output which is high if and only if m $\geq$1, AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m $\geq$k, and

elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m $\geq$1 and the number of high inputs is an odd number, AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m $\geq$k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.

22. [New] A logic circuit for multiplying two binary numbers, the logic circuit comprising:

an array generation logic adapted to generate an array of logical combinations of bits of binary numbers;

an array reduction logic adapted to reduce depth of the array to two binary numbers; and

an addition logic adapted to add the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs adapted to receive a plurality of binary inputs;

at least three outputs adapted to output binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and adapted to generate at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein said logic circuit comprises at least one of:

an elementary OR symmetric function logic comprising at least one of OR logic adapted to combine binary inputs to generate a binary output which is high if and only if m >1, and AND logic adapted to combine sets of binary inputs and OR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and

an elementary EXOR symmetric function logic comprising at least one of EXOR logic adapted to combine the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic adapted to combine sets of binary inputs and EXOR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said elementary EXOR symmetric function logic includes at least one of:

a logic to generate the least significant bit of the binary output;

a logic to generate the $(i+1)^{th}$ binary output including logic to AND logic combine 2^i of the binary inputs in each set and EXOR logic to combine the result of the AND logic combinations, where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance of a binary output.

23. [New] A logic circuit for multiplying two binary numbers, the logic circuit comprising:

an array generation logic adapted to generate an array of logical combinations of bits of the binary numbers;

an array reduction logic adapted to reduce the depth of the array to two binary numbers; and

an addition logic adapted to add the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs adapted to receive a plurality of binary inputs;

at least three outputs adapted to output binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and adapted to generate at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein said logic circuit comprises at least one of:

an elementary OR symmetric function logic comprising at least one of OR logic adapted to combine binary inputs to generate a binary output which is high if and only if m >1, and an AND logic adapted to combine sets of binary inputs and OR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and

an elementary EXOR symmetric function logic comprising at least one of EXOR logic adapted to combine the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and an AND logic adapted to combine sets of binary inputs and an EXOR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said elementary OR symmetric function logic includes logic to logically AND 2^{N-1} of the binary inputs in each set in the generation of the N^{th} binary output as the elementary OR symmetric function of the binary inputs, where N is the number of binary outputs and the N^{th} binary output is the most significant.

24. [New] A logic circuit for multiplying two binary numbers, the logic circuit comprising:

an array generation logic for generating an array of logical combinations of bits of the binary numbers;

an array reduction logic for reducing the depth of the array to two binary numbers; and

an addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein said logic circuit comprises at least one of:

an elementary OR symmetric function logic comprising at least one of OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and

an elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said elementary EXOR symmetric function logic is arranged to generate a first binary output as an elementary EXOR symmetric function of the binary inputs and said elementary OR symmetric function logic is arranged to generate an N^{th} binary output as an elementary OR symmetric function of the binary inputs.

25. [New] A logic circuit for multiplying two binary numbers, the logic circuit comprising:

array generation logic for generating an array of logical combinations of bits of the binary numbers;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein said logic circuit comprises at least one of:

elementary OR symmetric function logic comprising at least one of OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and

elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said elementary OR symmetric function logic includes intermediate logic to generate a plurality of possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, where N is the number of binary outputs, the sets used for each possible binary output being of different sizes which are a function of the binary output being generated; and selector logic to select one of the possible binary outputs based on at least one more significant binary output value.

26. [New] A logic circuit according to claim 25, wherein said intermediate logic includes logic to generate two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively, and said selector logic is arranged to select one of the possible binary outputs based on the N^{th} binary output value.

27. [New] A logic circuit for multiplying two binary numbers, the logic circuit comprising:

an array generation logic for generating an array of logical combinations of bits of the binary numbers;

an array reduction logic for reducing the depth of the array to two binary numbers; and

an addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein said logic circuit comprises at least one of:

elementary OR symmetric function logic comprising at least one of OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and

elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number,

where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said elementary OR symmetric function logic and said elementary EXOR symmetric function logic include a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary OR or EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

28. [New] A parallel counter comprising:

at least five input means for receiving a plurality of binary inputs;

at least three output means for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

logic means for receiving the plurality of binary inputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs; wherein the elementary OR symmetric function is a function of the OR logic combination of the binary inputs and is high if and only if $m \geq 1$, or the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if $m \geq k$; and the elementary EXOR symmetric function is a function of the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$ and the number of high inputs is an odd number, or the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.

29. [New] A parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the inputs and the outputs for receiving the plurality of binary inputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, said logic circuit comprising at least one of:

elementary OR symmetric function logic for generating at least one binary output as elementary OR symmetric functions of the binary inputs, and

elementary EXOR symmetric function logic for generating at least one binary output as elementary EXOR symmetric functions of the binary inputs;

wherein the elementary OR symmetric function is a function of the OR logic combination of the binary inputs and is high if and only if $m \geq 1$, or a function of the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if $m \geq k$; and the elementary EXOR symmetric function is a function of the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$ and the number of high inputs is an odd number, or a function of the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.